Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1 A method for fabricating a non-volatile memory cell structure, comprising:
providing a substrate having thereon a tunneling oxide layer, a floating gate layer and a dielectric layer;
etching the floating gate layer and the dielectric layer in order to define two floating gates;
forming a plurality of spacers on sidewalls of the floating gates;
oxidizing the substrate to grow a control gate oxide layer between the two floating gates and split gate oxide layer on an outer side of each of the two floating gates;
implanting ions into the substrate to form a drain between the two floating gates;
depositing a gate layer over the substrate, the gate layer covering the dielectric layer and the spacers;
forming a mask on the gate layer, the mask being disposed over the drain; and
etching the gate layer to form a control gate over the drain using the mask and simultaneously form a split gate at the outer side of each of the two floating gate in a self-aligned manner, wherein the split gate is opposite to the control gate.

[c2] 2. The method of claim 1 further comprising the following step:
implanting ions into the substrate to form two sources that are adjacent to the split gates.

[c3] 3. The method of claim 1 wherein the control gate extends to a top surface of the dielectric layer.

[c4] 4. The method of claim 3 wherein the control gate is isolated from the floating gates by the dielectric layer and the spacers, wherein the overlapping area between the control gate and each of the floating gates is greater than a top surface area of each of the floating gates.

[c5] 5. The method of claim 1 wherein the dielectric layer comprises a silicon oxide layer and a silicon nitride layer.

[c6] 6. The method of claim 1 wherein the spacer comprises a silicon oxide layer and a silicon nitride layer.

[c7] 7. The method of claim 1 wherein the gate layer is a polysilicon layer.